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10/584,733	05/25/2007	Kang-Chan Lee	CU-4904 WWP	8187

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LADAS & PARRY LLP
224 SOUTH MICHIGAN AVENUE
SUITE 1600
CHICAGO, IL 60604

EXAMINER	
YANG, I CHAN	
ART UNIT	PAPER NUMBER
2178	
MAIL DATE	DELIVERY MODE
10/26/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/584,733	LEE ET AL.	
	Examiner	Art Unit	
	I-CHAN YANG	2178	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2010* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the following communications: amendment filed on 8/13/2010, in which applicant have amended Claims 1-3, and cancelled Claims 7-9

- The objection to the Title has been withdrawn.
- The objections to the Drawing have been withdrawn.
- The objections to the Specification have been withdrawn.
- The objections of Claims 2 and 3 have been withdrawn.
- The rejection of Claims 7-9 under 35 USC §103 have been withdrawn.

Claims 1-6 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not

commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being obvious over *James et al.* (US 7,013,424, hereinafter, *James*) in view of *Ross* (US 7,305,615).

As per Claim 1: *James* discloses *an XML processor comprising* (*James*, Col 3, lines 33-42)*:*

receiving an XML document (*James*, Fig. 2B, step 32)*;*

a first memory storing software for performing an XML processing, variables, and values required to execute software on the received XML document (*James*, Fig. 4, storage 430, memory 4[2]8, Col 10, lines 14-17)*;*

a hardware processing module performing a part of the XML processing in a hardware manner on the received XML document (*James*, Fig. 4, special purpose processor 432, Col 10, lines 48-62), *and*

wherein the hardware processing module is separate and independent of the first memory [storing] the software for performing the XML processing (*James*, Fig. 4, special purpose processor is separate from the main memory)*;*

a CPU controlling the XML processing on the received XML document by the software stored in the first memory to generate the first output if the XML is executed by software, and to generate a second output if the part of the XML processing is

performed in the hardware manner (*James*, Fig 4, general purpose processor 412 and special purpose processor 432; Col 2, lines 52-61, Col 3, lines 22-58, XML processing can be performed by the general purpose processor, as done conventionally, or by the hardware-based special purpose processor),

wherein the XML processing time is reduced from the hardware processing module performing the part of the XML processing in the hardware manner (Col 3, lines 43-58, hardware implementation allows for speed-related improvements), *and*

wherein the first and second outputs are equivalent (Col 8, lines 32-49, the output of the XML processing, a parsed node tree representing the XML document, is the same regardless of whether the general purpose processor or the special purpose processor is used; the application process receiving the processed output is not modified to distinguish between the two possible outputs).

James does not appear to explicitly disclose

a second memory employed by the hardware processing module.

However, *Ross* discloses

a second memory employed by the hardware processing module (*Ross*, Fig. 5, parsing accelerator, Fig. 6, memory 601 employed by parsing accelerator, Col 6, lines 46-60).

At the time of the invention, it would have been obvious to one of ordinary skill in the art, to include additional memory, such as processor cache, in the dedicated XML processor. The motivation for doing so would have been to further optimize the XML processing by storing at least a portion of the processing data on the cache and avoid the more expensive processing time associated with data fetching operations from the main memory.

As per Claim 2: The combination of *James* and *Ross* discloses *the XML processor according to claim 1, wherein the hardware processing module performs a memory management function used in XML parsing from at least one of assignment, return, and reassignment of memory among XML processing functions* (Col 7, lines 21-23, dedicated XML processor creates DOM for parsed XML; Col 5, line 63 thru Col 6, line10, DOM creation includes memory management operations).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being obvious over *James* in view of *Ross* and further in view of *Hind et al.* (US 6,938,204, hereinafter, *Hind*).

As per Claim 3: The combination of *James* and *Ross* discloses *the XML processor according to claim 2, wherein the hardware processing module processes the assignment, the reassignment, and the return of memory with respect to XML elements which are expressed as nodes and a tree relation between the nodes* (*James*, Col 6,

lines 1-10, memory allocation, de-allocation, and reclamation for objects within XML hierarchical structure).

The combination of *James* and *Ross* does not appear to explicitly disclose

a node usage check table divided into several blocks, each block indicating whether to use a corresponding node table;

a node table managing the whole information that each node has to store, at least one of a node name, a node type, a parent node, a child node; and

a node memory storing actual content of every component of the node table.

However, *Hind* discloses an array based storage format for XML data, and further discloses

a node usage check table divided into several blocks, each block indicating whether to use a corresponding node table (*Hind*, Fig. 5C, 520, Col 13, lines 26-36, the attribute array is a node usage check table divided into several blocks, each block indicating whether a corresponding secondary array is used)*;*

a node table managing the whole information that each node has to store, at least one of a node name, a node type, a parent node, a child node (*Hind*, Fig. 5C, 530 and 540, Col 13, lines 36-40, the secondary array is a node table managing the whole attribute information each node has to store)*; and*

a node memory storing actual content of every component of the node table (Fig. 5C, Fig. 4C, Col 13, line 54 thru Col 14, line 5, data buffer 480 in Fig. 4C is a node memory storing actual content of every component from the secondary array).

At the time of the invention, it would have been obvious to one of ordinary skill in the art, to include *Hind*'s array-based storage format for XML data in the combination of *James* and *Ross*. The feasibility and desirability of such combination is further evident in the incorporation of *Hind* by reference in the Specification of *James* (*James*, Col 6, lines 25-30). The motivation for the combination would have been to realize further performance gains by implementing the array-based processing for faster navigation of the tree structure (*James*, Col 6, lines 11-25).

As per Claim 4: The combination of *James, Ross,* and *Hind* discloses *the XML processor according to claim 3, wherein the node table has addresses in which every component on the node memory is respectively stored* (*Hind*, Col 13, lines 40-50, secondary array has references/addresses in the form of a data buffer pointer, a offset from the beginning of the data buffer, and a data length for every attribute component).

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being obvious over *James* in view of *Ross* and further in view of *Dapp et al.* (US 7,080,094, hereinafter, *Dapp*).

As per Claim 5: The combination of *James* and *Ross* does not appear to explicitly disclose

wherein the hardware processing module performs an XML DTD processing.

However, *Dapp* discloses a hardware XML processing module that performs XML DTD processing (*Dapp*, Col 3, lines 27-28, hardware XML accelerator, Col 2, lines 18-25, DTD or XML schema validation).

At the time of the invention, it would have been obvious to one of ordinary skill in the art, to perform DTD processing with the dedicated XML processor. The motivation for doing so would have been to use a specialized XML processor for resource-intensive XML validation operations (*Dapp*, Col 2, line 55 thru Col 3, line 2).

As per Claim 6: The combination of *James* and *Ross* does not appear to explicitly disclose

wherein the hardware processing module performs a state machine of an XML schema.

However, *Dapp* discloses a hardware XML processing module that *performs a state machine of an XML schema* (*Dapp*, Col 2, lines 37-41).

At the time of the invention, it would have been obvious to one of ordinary skill in the art, to perform XML validation processing including state machine implementation with the dedicated XML processor. The motivation for doing so would have been to use a specialized XML processor for resource-intensive XML validation operations (*Dapp*, Col 2, line 55 thru Col 3, line 2).

Response to Arguments

Applicant's arguments filed 8/13/2010 have been fully considered but they are not persuasive.

Specifically, the Applicant has argued, on page 11, 12, and 13 or the Remarks, that the cited references do not disclose a separate and independent hardware-based XML processor to perform the XML processing in a hardware manner.

The examiner respectfully disagrees. As disclosed in numerous locations within the disclosure of the primary reference, James does disclose a dedicated, special purpose XML processor implemented in a hardware manner to further provide speed-related advantages (Col 3, lines 43-58, Col 5, 24-35, Col 8, lines 41-49).

Accordingly, the same grounds of rejection with additional clarifications for the newly amended limitations are maintained for the independent claim 1 and its dependent claims 2-6.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to I-Chan Yang whose telephone number is (571) 270-3840. The examiner can normally be reached on Monday - Friday, 9:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Hong can be reached on (571) 272-4124. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen S. Hong/
Supervisory Patent Examiner, Art Unit 2178

/I. Y./
Examiner, Art Unit 2178